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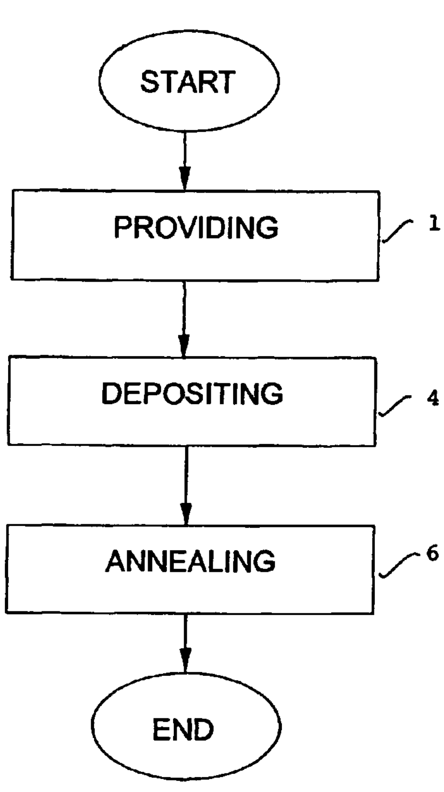
(54) Title: METHOD FOR FORMING A NICKEL SILICIDE LAYER ON A SILICON SUBSTRATE



(57) Abstract: A method for forming nickel silicide on a silicon substrate wherein silicon oxide, if present on the substrate, does not substantially inhibit the formation of the nickel silicide. The method is particularly useful in the formation of CMOS transistors and includes a number of steps. The first step (1) involves providing a silicon substrate having a surface. The next step (4) involves depositing a layer of nickel alloy on the substrate surface, the nickel alloy being made from nickel and an oxide-reacting material such as Titanium or Tantalum. The next step (6) involves annealing the nickel alloy layer and the substrate causing the nickel in the nickel alloy layer to react with the silicon substrate and form a nickel silicide layer on the substrate surface. By using a nickel alloy containing an oxide-reacting material, silicon oxide, if present on the substrate surface, does not substantially inhibit the formation of the nickel silicide layer.

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METHOD FOR FORMING A NICKEL SILICIDE LAYER ON A SILICON SUBSTRATE

Technical Field

The present invention relates to methods for forming nickel silicide on silicon substrates and, in particular, relates to a method for forming nickel silicide on a silicon substrate wherein silicon oxide, if present on the substrate, does not substantially inhibit the formation of the nickel silicide.

Background Art

When forming contacts on the source, drain, and gate regions of complementary metal-oxide-semiconductor (CMOS) transistors, it is common to simultaneously form self-aligned silicide (or salicide) on the source, drain, and gate regions. Silicides allow for high-speed device operation by reducing resistance-capacitance (RC) time delay and constitute stable, low-resistance contacting structures. In this way, they help minimize source/drain series resistance and optimise device performance.

Titanium (Ti) and cobalt (Co) silicides are the most commonly used silicides. However, it is difficult to form a low resistivity phase on narrow lines using titanium silicide. In addition, the use of cobalt silicide often results in large silicon consumption as well as high junction leakage. In addition, in order to form Ti and Co silicides the materials need to be annealed at temperatures around 700°C.

An alternative silicide which can also be used in the silicide process is nickel monosilicide (NiSi). NiSi has a low resistance (15-18 $\mu\Omega$ cm) and can be formed at temperatures in the range of 400°C to 700°C. In contrast to conventional titanium silicide, the sheet resistance of NiSi is not affected by strong linewidth effects. An advantage NiSi has over cobalt silicide is that for the same silicide thickness, Si consumption for its formation is only 80 % of that for cobalt silicide. The lower Si consumption of NiSi is particularly

advantageous for its use in devices with ultra small feature sizes since this alleviates the stringent constraints on salicide processes that result from junction depth scaling with low resistance requirements.

However, there are two major concerns for the use of NiSi. Like $CoSi_2$, NiSi is sensitive to oxygen contamination from the ambient air and from residual interfacial contaminants such as native oxides. Such contamination can lead to rough interfaces and high diode leakage on shallow junctions.

The presence of such native oxides on a silicon substrate substantially inhibit the formation of nickel silicides. This is because the native oxide acts as a diffusion barrier, preventing the nickel from reacting with the silicon. The formation of nickel silicide often fails in the presence of native oxide. In this case, although nickel silicide formation may be achieved using high processing temperature, e.g., 700°C or above, the silicide formed is dilicide with higher resistivity, but not the desired monosilicide with low resistivity.

The present invention provides a method for forming nickel silicide on a silicon substrate wherein silicon oxide, if present on the substrate, does not substantially inhibit the formation of the nickel silicide.

Disclosure of Invention

In a first aspect, the present invention provides a method for forming a nickel silicide layer on a silicon substrate comprising the steps of:

(a) providing a silicon substrate having a surface;

(b) depositing a layer of nickel alloy on the substrate surface, the nickel alloy comprising nickel and an oxide-reacting material; and

(c) annealing the nickel alloy layer and the substrate causing the nickel in the nickel alloy layer to react with the silicon substrate and form a nickel silicide layer on the substrate surface and wherein silicon oxide, if present on the surface, does not substantially inhibit the formation of the nickel silicide layer.

Preferably, the nickel alloy layer, once deposited, has an exposed surface and wherein the oxide-reacting material in the nickel alloy substantially inhibits the formation of nickel oxides on the exposed surface.

Preferably, the oxide-reacting material is selected from the group consisting of:

(a) Titanium; and

(b) Tantalum.

Preferably, the nickel alloy layer comprises 80-98% nickel and 2-20% oxide-reacting material. More preferably, the nickel alloy layer comprises about 95% nickel and about 5% oxide-reacting material.

Preferably, the step of annealing the layer and the substrate comprises annealing at temperatures ranging from about 400°C to 700°C. More preferably, the step of annealing the layer and the substrate comprises annealing at temperatures ranging from about 450°C to 550°C.

Preferably, the step of depositing the layer of the nickel alloy on the substrate surface comprises depositing the layer by a technique selected from:

(a) sputtering;

(b) e-beam evaporation; and

(c) thermal evaporation.

Alternatively, the step of providing a silicon substrate having a surface comprises the steps of:

(a) providing a silicon substrate having a surface; and

(b) growing a layer of chemical oxide on the substrate surface.

Preferably, the step of growing the layer of chemical oxide on the substrate surface comprises growing a layer of silicon oxide to a thickness of about 5-20Å. More preferably, the step of growing the layer of silicon oxide on the substrate surface comprises growing the layer to a thickness of about 12-13Å.

Preferably, the annealing step comprises annealing the nickel alloy layer, the chemical oxide layer and the substrate thereby causing:

(i) the oxide-reacting material in the nickel alloy layer to react with the chemical oxide layer to form a diffusion membrane on the substrate surface, the diffusion membrane being formed from the reaction between the oxide-reacting material and the chemical oxide; and

(ii) nickel atoms from the nickel alloy layer to diffuse through the diffusion membrane and react with the silicon substrate to form a nickel silicide layer on the substrate surface, beneath the diffusion membrane.

Preferably, the nickel atoms diffuse through the diffusion membrane substantially uniformly.

Preferably, the nickel silicide layer is a substantially flat nickel silicide layer.

In a second aspect, the present invention provides a modified silicon substrate comprising a silicon substrate having a surface and a layer of nickel silicide on the substrate surface, the modified substrate having been formed by the first aspect of the present invention.

In a third aspect, the present invention provides a modified silicon substrate comprising:

(a) a silicon substrate having a surface;

(b) a layer of nickel silicide on the substrate surface, the nickel silicide layer having been formed by:

(i) depositing a layer of nickel alloy on the substrate surface the nickel alloy comprising nickel and an oxide-reacting material; and

(ii) annealing the nickel alloy layer and the substrate, thereby causing the nickel alloy layer to react with the substrate to form the nickel silicide layer on the substrate surface

wherein silicon oxide, if present on the surface, does not substantially inhibit the formation of the nickel silicide layer.

Preferably, the oxide-reacting material is selected from the group consisting of:

(a) Titanium; and

(b) Tantalum.

Preferably, the nickel alloy layer comprises 80-98% nickel and 2-20% oxide-reacting material. More preferably, the nickel alloy layer comprises about 95% nickel and about 5% oxide-reacting material.

Preferably, the nickel silicide layer was formed by annealing the nickel alloy layer and the substrate at temperatures ranging from 400°C to 700°C. More preferably, the nickel silicide layer was formed by annealing the nickel alloy layer and the substrate at temperatures ranging from 450°C to 550°C.

Preferably, the nickel silicide layer was formed by depositing the layer of the nickel alloy on the substrate surface by a technique selected from:

(a) sputtering;

(b) e-beam evaporation; and

(c) thermal evaporation.

Alternatively, the nickel silicide layer was formed by:

(a) providing a silicon substrate having a surface; and

(b) growing a layer of chemical oxide on the substrate surface

prior to depositing the layer of nickel alloy on the substrate surface and annealing the nickel alloy layer, the chemical oxide layer and the substrate.

Preferably, the nickel silicide layer was formed by growing the layer of chemical oxide on the substrate surface to a thickness of 5 to 20Å. More preferably, the nickel silicide layer was formed by growing the layer of chemical oxide on the substrate surface to a thickness of about 12 to 13Å.

Preferably, the nickel silicide layer was formed by annealing the nickel alloy layer, the chemical oxide layer and the substrate thereby causing:

(i) the oxide-reacting material in the nickel alloy layer to react with the chemical oxide layer to form a diffusion membrane on the substrate surface, the diffusion membrane being formed from the reaction between the oxide-reacting material and the chemical oxide; and

(ii) nickel atoms from the nickel alloy layer to diffuse through the diffusion membrane and react with the silicon substrate to form a nickel silicide layer on the substrate surface, beneath the diffusion membrane.

Preferably, the nickel silicide layer was formed by the nickel atoms diffusing through the diffusion membrane substantially uniformly.

Preferably, the nickel silicide layer is a substantially flat nickel silicide layer.

Throughout this specification, unless the context requires otherwise, the word "comprise", or variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated element, integer or step, or group of elements, integers or steps, but not the exclusion of any other element, integer or step, or group of elements, integers or steps.

Any discussion of documents, acts, materials, devices, articles or the like which has been included in the present specification is solely for the purpose of providing a context for the present invention. It is not to be taken as an admission that any or all of these matters form part of the prior art base or were common general knowledge in the field relevant to the present invention as it existed before the priority date of each claim of this application.

In order that the present invention may be more clearly understood, preferred forms will be described with reference to the following drawings and examples.

Brief Description of the Drawings

Figure 1 is a flow chart illustrating a first preferred method according to the invention;

Figures 2-4 are cross-sectional side views of a silicon substrate having a nickel silicide layer formed thereon according to the first preferred method of the present invention;

Figure 5 is a flow chart illustrating a second preferred method according to the present invention;

Figures 6-9 are cross-sectional side views of a silicon substrate having a nickel silicide layer formed thereon according to the second preferred method of the present invention; and

Figures 10-13 are cross-sectional side views of a complementary metal-oxide-silicon (CMOS) transistor having a layer of nickel silicide formed thereon according to the first preferred method of the present invention.

Detailed Description

Referring to Figure 1, there is shown a flow chart illustrating the first preferred method for forming a nickel silicide layer on a silicon substrate according to the present invention. As shown in Figures 1 and 2 the first step involves providing 1 a silicon substrate 2 having a surface 3.

As shown in Figures 1 and 3, the next step involves depositing 4 a layer of nickel alloy 5 on the substrate surface 2. The nickel alloy is made up of nickel and an oxide reacting material such as titanium or tantalum. The following description assumes that the nickel alloy is nickel titanium (Ni(Ti)). In this preferred embodiment the nickel alloy is made from about 95% nickel and about 5% titanium. Alternative compositions in which nickel comprises about 80% to 98% of the nickel alloy and titanium comprises about 2% to 20% of the nickel alloy may also be used.

The nickel alloy layer 5 is preferably deposited on the substrate 2 by sputtering, e-beam evaporation or thermal evaporation to a thickness of about 5 to 50 nm.

As shown in Figures 1 and 4, the next step involves annealing 6 the nickel alloy layer 5 and the substrate 2. During the annealing step any residual silicon dioxide (SiO_2) on the substrate surface 3 reacts with the titanium in the nickel alloy layer 5 to form a titanium silicon oxide ($Ti_xSi_yO_z$, where x, y and z are integers greater than or equal to 1) diffusion membrane 8. The diffusion membrane 8 allows a flux of nickel atoms to diffuse from the nickel alloy layer 5 through the diffusion membrane 8 into the silicon substrate 2. As the nickel atoms diffuse through the diffusion membrane they react with the silicon substrate 2 to form a layer of nickel silicide 7. This nickel silicide layer 5 forms beneath the diffusion membrane 8. The effective reduction of residual oxide, if any, through the mechanism stated above assures the formation of nickel silicide even in the presence of residual oxide at low processing temperatures (e.g., 450 to 500 °C), thus improving manufacturing yield.

The resulting structure, as shown in Figure 4, comprises a silicon substrate 2 upon which a substantially flat nickel silicide layer 7 is formed. The nickel silicide layer has a thin $Ti_xSi_yO_z$ diffusion membrane 8 on top of it. The unreacted portion of the nickel alloy layer 5 remains on top of the diffusion membrane 8.

The step of annealing 6 the nickel alloy layer 5 and the silicon substrate 2 should be performed at temperatures ranging from about 450°C to 550°C. Temperatures ranging from about 400°C to 700°C may also be used. It will be appreciated by those skilled in the art that these temperatures are much less than those conventionally needed to form nickel silicide (typically around 700°C) when residual silicon oxides are present.

Figure 5 shows a flow chart illustrating a second preferred method according to the present invention. The main difference between this preferred method and the previous preferred method is that this method includes an additional step of growing a layer of chemical oxide on the substrate surface. When this chemical oxide reacts with the titanium in the nickel alloy layer a

substantially uniform diffusion membrane is formed which facilitates the formation of a substantially flat nickel silicide layer beneath it. The steps and features indicated in Figures 5-9 which have the same numerical reference as those indicated in Figures 1 to 4 are intended to refer to common steps or features.

As shown in Figures 5 and 6, the first step in this second preferred method involves providing 1 a silicon substrate 2 having a surface 3.

Referring to Figures 5 and 7, the next step involves growing 9 a layer of chemical oxide 10 on the substrate surface. The layer of chemical oxide 10 is preferably a layer of silicon oxide grown to a thickness of about 12-13 Å. Thicknesses of about 5-20Å may also be used. Before growing the thin chemical oxide layer 10, the substrate 2 may be cleaned by immersion in HF.

As shown in Figures 5 and 8, the next step involves depositing 4 a layer of nickel alloy 5 on the substrate surface 2. As described above with reference to the first preferred method, the nickel alloy is made up of nickel and an oxide reacting material such as titanium or tantalum. The following description assumes that the nickel alloy is nickel titanium (Ni(Ti)).

As shown in Figures 5 and 9, the next step involves annealing 6 the nickel alloy layer 5 and the substrate 2. During the annealing step the layer of silicon oxide 10 on the substrate surface 3 reacts with the titanium and the nickel alloy layer 5 to form a titanium silicon oxide ($Ti_xSi_yO_z$ where x, y and z are integers greater than or equal to 1) diffusion membrane 8. As described above, the diffusion membrane 8 allows a flux of nickel atoms to diffuse from the nickel alloy layer 5 through the diffusion membrane 8 into the silicon substrate 2. The reactions which take place and the resulting structure, shown in Figure 9, are substantially the same as those described with reference to Figures 1 and 4 above.

One of the advantages of both of the above methods is that the diffusion membrane 8 allows the silicidation reaction to take place slowly. This slow reaction rate results in a very smooth interface between the silicon substrate 2 and the nickel silicide layer 7. When used in very shallow junctions, the smooth

silicide/silicon interface greatly reduces the potential for current leakage. Furthermore, because the nickel silicide layer 7 exhibits reduced grooving at the grain boundary this results in enhanced agglomeration resistance and improves the thermal stability of the nickel silicide film.

Figures 10 to 13 illustrate the application of the first preferred method in forming a nickel silicide layer on the source 13, gate 20 and drain regions 14 of a complimentary metal-oxide-silicon (CMOS) transistor 11.

As shown in Figures 1 and 10, the first step involves providing 1 a partially formed transistor 11 including a silicon substrate 2, a number of insulating regions 12 and a number of bared source, drain and gate regions 13, 14, 20.

Turning to Figures 1 and 11, the next step involves depositing 4 a layer of nickel alloy 5 on the substrate. The layer of nickel alloy is deposited by sputtering, e-beam evaporation or thermal evaporation to a thickness of about 5 to 50 nm. The nickel alloy layer covers the insulating regions 12 and source, gate and drain regions 13 14, 20 of the partially formed transistor 11.

Turning to Figures 1 and 12, the next step involves annealing 6 the entire transistor at temperatures ranging from about 450°C to 550°C. Temperatures ranging from about 400°C to 700°C may also be used. During the annealing step any residual silicon dioxide (S_iO_2) on the source gate and drain regions 13,14, 20 reacts with the titanium in the nickel alloy layer 5 to form a titanium-silicon-oxide diffusion membrane 8. As with previous examples, the diffusion membrane 8 allows a flux of nickel atoms to diffuse from the nickel alloy layer 5 through the diffusion membrane 8 into the source, gate and drain regions 13, 14 of the silicon substrate 2. As the nickel atoms diffuse through the diffusion membrane 8, they react with the silicon substrate 2 to form a layer of nickel silicide 7. The portions of the nickel alloy layer 5 on the insulating regions 12 are unable to react with the silicon substrate 2 due to the presence of the insulating regions 12.

The resulting structure, as shown in Figure 12, comprises a transistor 11 having a number of source, gate and drain regions 13, 14, 20 upon which a

substantially flat nickel silicide layer 7 is formed. That layer has a thin $Ti_xSi_yO_z$ diffusion membrane 8 on top of it. The unreacted portion of the nickel alloy layer 5 on the source gate and drain regions 13, 14 remains on top of the diffusion membrane 8.

As shown in Figure 13, the last step in the process involves etching off the unreacted nickel alloy layer 5 and the diffusion membrane 8 using an appropriate chemical etchant to leave a transistor 11 having source gate and drain regions 13 with a substantially flat layer of nickel silicide 7 formed thereon.

Although this CMOS transistor application has been described with reference to the first preferred method, the second preferred method, involving the step of growing a layer of chemical oxide on the source, gate and drain regions, may also be used.

It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

Claims:

1. A method for forming a nickel silicide layer on a silicon substrate comprising the steps of:

(a) providing a silicon substrate having a surface;

(b) depositing a layer of nickel alloy on the substrate surface, the nickel alloy comprising nickel and an oxide-reacting material;

(c) annealing the nickel alloy layer and the substrate causing the nickel in the nickel alloy layer to react with the silicon substrate and form a nickel silicide layer on the substrate surface and wherein silicon oxide if present on the surface does not substantially inhibit the formation of the nickel silicide layer.

2. A method according to claim 1 wherein, once deposited, the nickel alloy layer has an exposed surface and wherein the oxide-reacting material in the nickel alloy substantially inhibits the formation of nickel oxides on the exposed surface.

3. A method according to claim 1 or claim 2 wherein the oxide-reacting material is selected from the group consisting of:

(a) Titanium; and

(b) Tantalum.

4. A method according to any one of the preceding claims wherein the nickel alloy layer comprises 80 to 98% nickel and 2 to 20% oxide-reacting material.

5. A method according to claim 4 wherein the nickel alloy layer comprises about 95% nickel and about 5% oxide-reacting material.

6. A method according to any one of preceding claims wherein the step of annealing the layer and the substrate comprises annealing at temperatures ranging from 400°C to 700°C.

7. A method according to claim 6 wherein the step of annealing the layer and the substrate comprises annealing at temperatures ranging from 450°C to 550°C.

8. A method according to any one of the preceding claims wherein the step of depositing the layer of the nickel alloy on the substrate surface comprises depositing the layer by a technique selected from:

(a) sputtering;

(b) e-beam evaporation; and

(c) thermal evaporation.

9. A method according to any one of the preceding claims wherein the step of providing a silicon substrate having a surface comprises the steps of:

(a) providing a silicon substrate having a surface; and

(b) growing a layer of chemical oxide on the substrate surface.

10. A method according to claim 9 wherein the step of growing the layer of chemical oxide on the substrate surface comprises growing a layer of silicon oxide to a thickness of 5 to 20Å.

11. A method according to claim 10 wherein the step of growing the layer of silicon oxide on the substrate surface comprises growing the layer to a thickness of 12 to 13Å.

12. A method according to any one of claims 9 to 11 wherein the annealing step comprises annealing the nickel alloy layer, the chemical oxide layer and the substrate thereby causing:

(i) the oxide-reacting material in the nickel alloy layer to react with the chemical oxide layer to form a diffusion membrane on the substrate surface, the diffusion membrane being formed from the reaction between the oxide-reacting material and the chemical oxide; and

(ii) nickel atoms from the nickel alloy layer to diffuse through the diffusion membrane and react with the silicon substrate to form a nickel silicide layer on the substrate surface, beneath the diffusion membrane.

13. A method according to claim 12 wherein the nickel atoms diffuse through the diffusion membrane substantially uniformly.

14. A method according to claim 12 or claim 13 wherein the nickel silicide layer is a substantially flat nickel silicide layer.

15. A modified silicon substrate comprising a silicon substrate having a surface and a layer of nickel silicide on the substrate surface, the modified substrate having been formed by the method defined in any one of claims 1 to 14.

16. A modified silicon substrate comprising:

(a) a silicon substrate having a surface;

(b) a layer of nickel silicide on the substrate surface, the nickel silicide layer having been formed by:

(i) depositing a layer of nickel alloy on the substrate surface, the nickel alloy comprising nickel and an oxide-reacting material; and

(ii) annealing the nickel alloy layer and the substrate, thereby causing the nickel alloy layer to react with the substrate to form the nickel silicide layer on the substrate surface wherein silicon oxide if present on the surface, does not substantially inhibit the formation of the nickel silicide layer.

17. A modified silicon substrate according to claim 16 wherein the oxide-reacting material is selected from the group consisting of:

(a) Titanium; and

(b) Tantalum.

18. A modified silicon substrate according to claim 16 or claim 17 wherein the nickel alloy layer comprises 80 to 98% nickel and 2 to 20% oxide-reacting material.

19. A modified silicon substrate according to claim 18 wherein the nickel alloy layer comprises about 95% nickel and about 5% oxide-reacting material.

20. A modified silicon substrate according to any one of claims 16 to 19 wherein the nickel silicide layer was formed by annealing the nickel alloy layer and the substrate at temperatures ranging from 400°C to 700°C.

21. A modified silicon substrate according to claim 20 wherein the nickel silicide layer was formed by annealing the nickel alloy layer and the substrate at temperatures ranging from 450°C to 550°C.

22. A modified silicon substrate according to any one of claims 16 to 21 wherein the nickel silicide layer was formed by depositing the layer of the nickel alloy on the substrate surface by a technique selected from:

(a) sputtering;

(b) e-beam evaporation; and

(c) thermal evaporation.

23. A modified silicon substrate according to any one of claims 16 to 22 wherein the nickel silicide layer was formed by:

(a) providing a silicon substrate having a surface; and

(b) growing a layer of chemical oxide on the substrate surface

prior to depositing the layer of nickel alloy on the substrate surface and annealing the nickel alloy layer, the chemical oxide layer and the substrate.

24. A modified silicon substrate according to claim 23 wherein the nickel silicide layer was formed by growing the layer of chemical oxide on the substrate surface to a thickness of 5 to 20Å.

25. A modified silicon substrate according to claim 24 wherein the nickel silicide layer was formed by growing the layer of chemical oxide on the substrate surface to a thickness of about 12 to 13Å.

26. A modified silicon substrate according to any one of claims 23 to 25 wherein the nickel silicide layer was formed by annealing the nickel alloy layer, the chemical oxide layer and the substrate thereby causing:

(i) the oxide-reacting material in the nickel alloy layer to react with the chemical oxide layer to form a diffusion membrane on the substrate surface, the diffusion membrane being formed from the

reaction between the oxide-reacting material and the chemical oxide; and

(ii) nickel atoms from the nickel alloy layer to diffuse through the diffusion membrane and react with the silicon substrate to form a nickel silicide layer on the substrate surface, beneath the diffusion membrane.

27. A modified silicon substrate according to claim 26 wherein the nickel silicide layer was formed by the nickel atoms diffusing through the diffusion membrane substantially uniformly.

28. A modified silicon substrate according to any one of claims 16 to 27 wherein the nickel silicide layer is a substantially flat nickel silicide layer.

29. A method for forming a nickel silicide layer on a silicon substrate substantially as described herein with reference to the accompanying figures and examples.

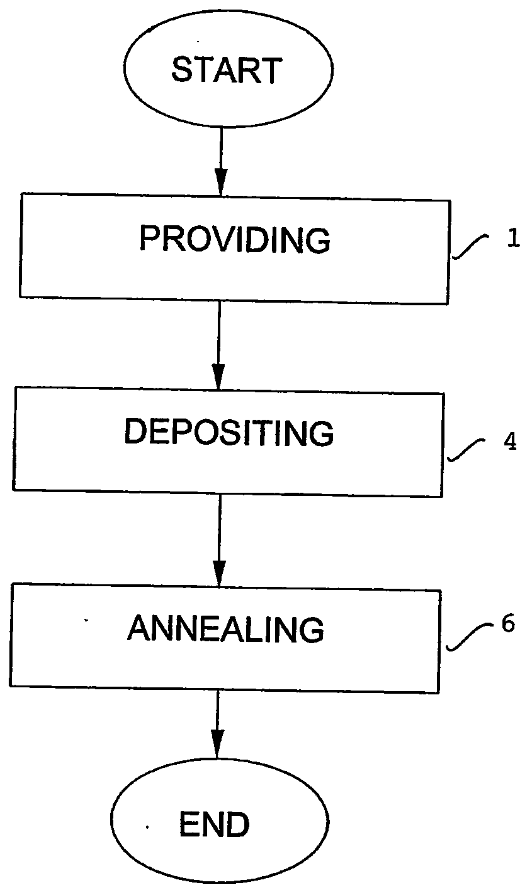

FIG. 1

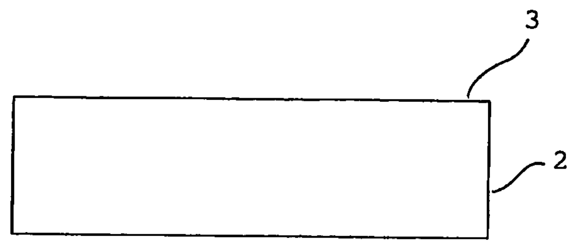

FIG. 2

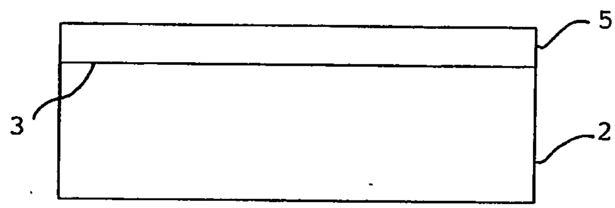

FIG. 3

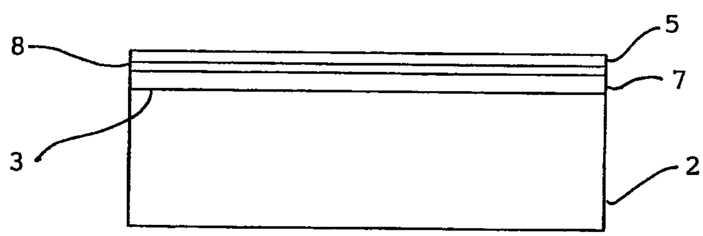

FIG. 4

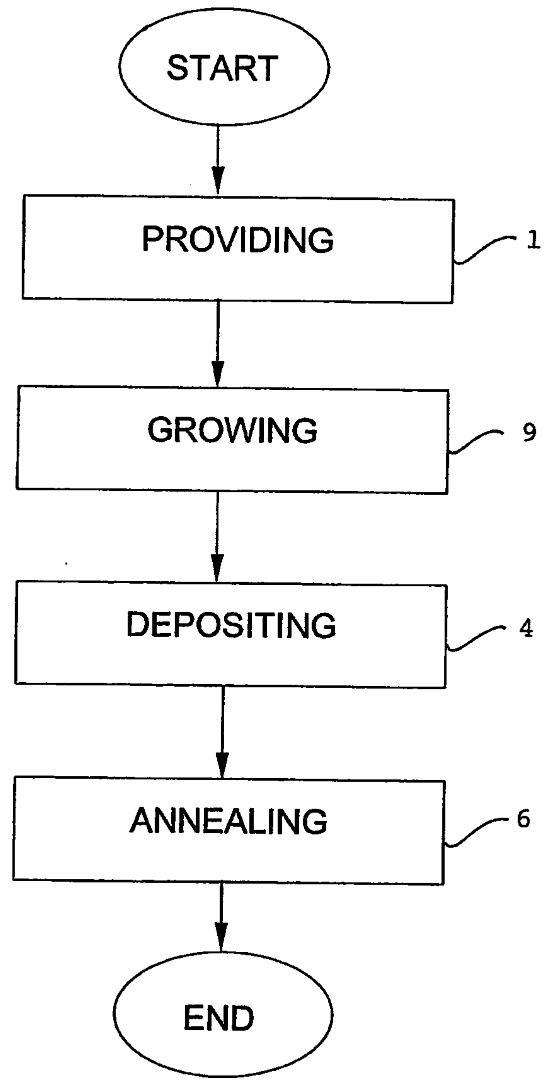

FIG. 5

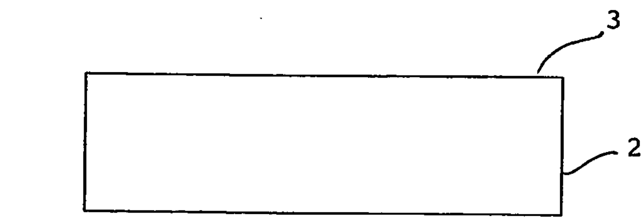

FIG. 6

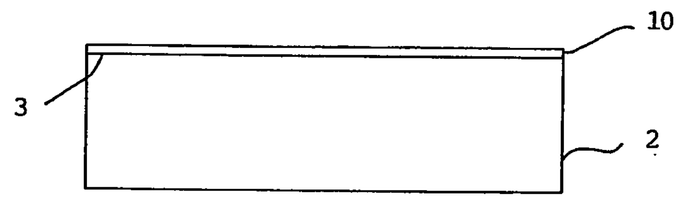

FIG. 7

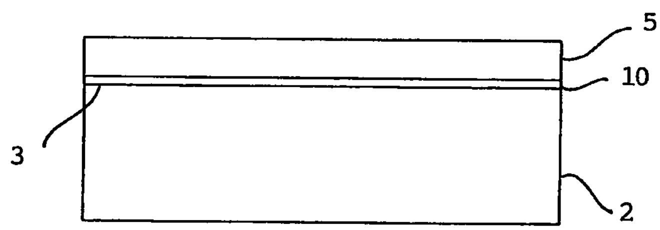

FIG. 8

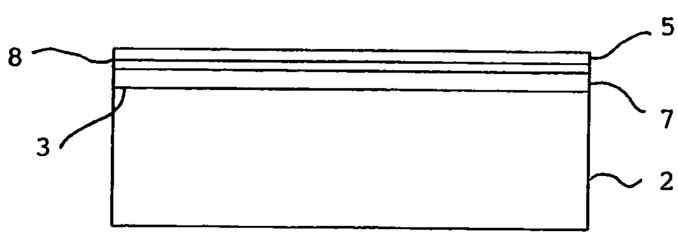

FIG. 9

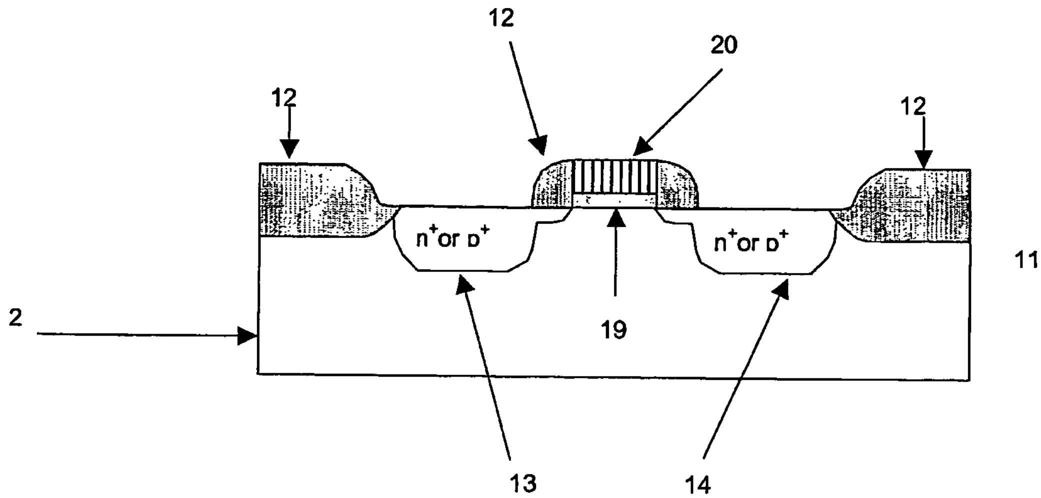
12
20
12
12
n+or p+
n+or p+
11
2
19
13
14

FIG. 10

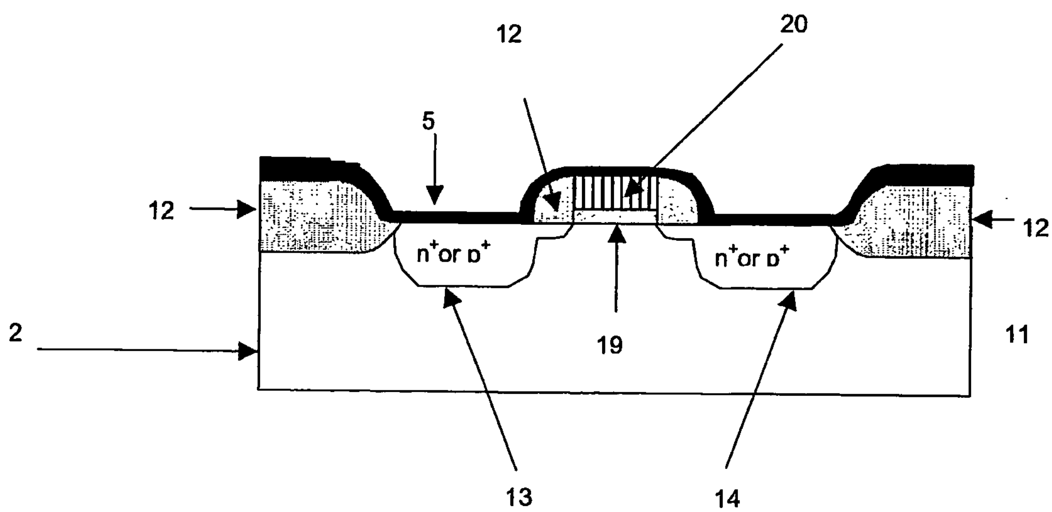
12
20
5
12
12
n+or p+
n+or p+
2
19
11
13
14

FIG. 11

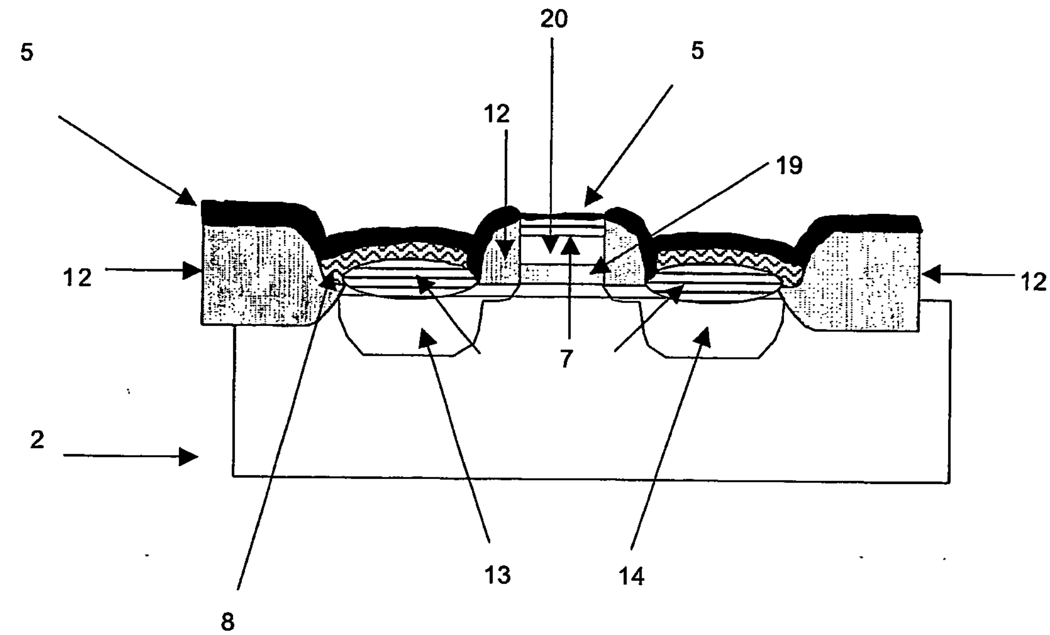

FIG. 12

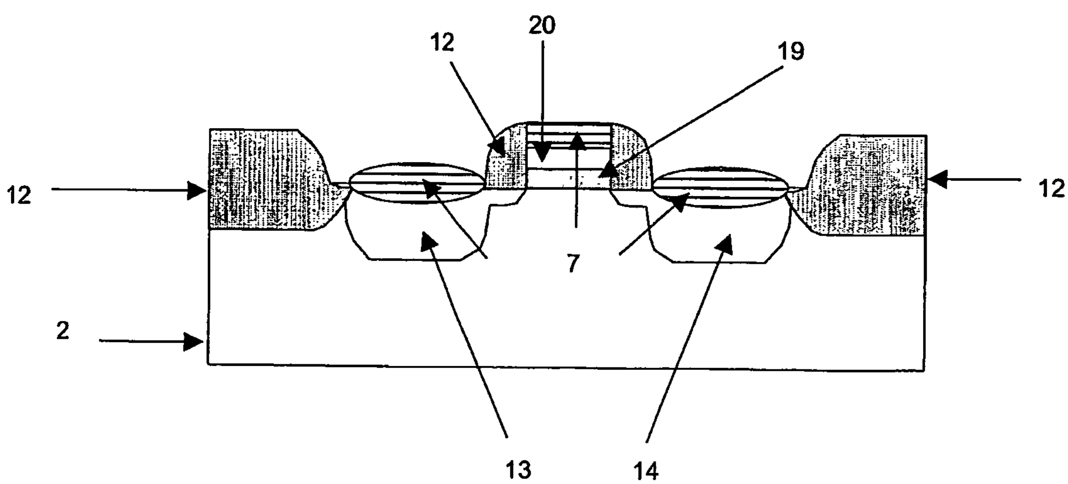

FIG. 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG03/00096

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. 7: H01L 21/44, 21/283, 21/24, 21/4763, 29/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI: H01L/ic,+silicon or Si, (nickel or Ni+)(2d)(+silicid+ or +salicid+ or NiSi),+oxid?? or oxygen+ or SiO+ or silica, (nickel or Ni+)(s)(alloy? or metal? or Titanium or Tantalum or Ti+ or Ta+), anneal+ or heat+ or temper+, (nickel or Ni or NiSi+)(s)(layer? or film? or membrane? or sheet? or deposit+ or coat+), diffus+, +uniform+ or flat or smooth+ or rough+ or +homoge+ or +even+ or irregular

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, X	US 6440851 B1 (AGNELLO et al.) 27 August 2002 Abstract, column 2, line 32 - column 4, line 56	1-8, 15-22, 28-29
P, X	US 20020151170 A1 (MAEX et al.) 17 October 2002 Abstract, paragraphs 9, 11, 14, 19, 21, 64 and 86-89	1-8, 15-22, 28-29
A	US 6303504 B1 (LIN) 16 October 2001 Abstract, column 1, line 27- column 2, line 67	1-8, 15-22, 28-29

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search	Date of mailing of the international search report
27 June 2003	11 JUL 2003

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG03/00096

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6339021 B1 (TAN et al.) 15 January 2002 Abstract, column 1, line 12 - column 2, 24, column 3, line 9 - column 4, line 64	1-8, 15-22, 18-29
A	US 20020045344 A1 (WANG et al.) 18 April 2002 Abstract, paragraphs 3, 10, 20, 28, claims 6-7, 23	1-8, 15-22, 18-29
A	US 5668040 A (BYUN) 16 September 1997 Abstract, column 3, lines 29 - 42, column 4, lines 11-15, column 5, lines 13-26 and 45-67	1-8, 15-22, 18-29
P, A	US 20020068408 A1 (PATON et al.) 6 June 2002 Abstract, paragraphs 3-5, 8-12, 34, 36 and 39	1-8, 15-22, 18-29
P, A	US 6495460 B1 (BERTRAND et al.) 17 December 2002 Abstract, column 2, line 33- column 3, line 58, column 5, line 20 - column 7, line 54	1-8, 15-22, 18-29

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG03/00096

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member			
US	6440851	US	2002182836		
US	2002151170	US	5780362	US	2002045344
US	6303504	NONE			
US	6339021	NONE			
US	2002045344	US	5780362	US	2002151170
US	5668040	JP	8264481		
US	2002068408	AU	200230565	WO	200247145
US	6495460	NONE			

END OF ANNEX

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

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International Bureau

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(26) Publication Language: English

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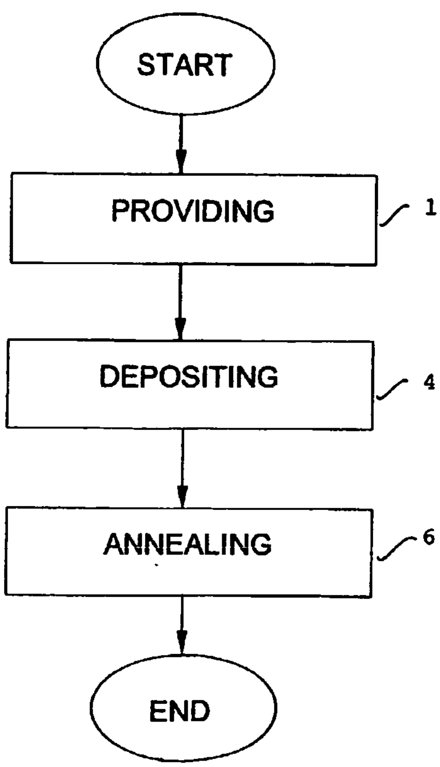
(74) Agents: **KOH, Patsy** et al.; Arthur Loke & Partners, 9, Temasek Boulevard #23-01, Suntec Tower Two, Singapore 038989 (SG).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD,

[Continued on next page]

(54) Title: METHOD FOR FORMING A NICKEL SILICIDE LAYER ON A SILICON SUBSTRATE



(57) Abstract: A method for forming nickel silicide on a silicon substrate wherein silicon oxide, if present on the substrate, does not substantially inhibit the formation of the nickel silicide. The method is particularly useful in the formation of CMOS transistors and includes a number of steps. The first step (1) involves providing a silicon substrate having a surface. The next step (4) involves depositing a layer of nickel alloy on the substrate surface, the nickel alloy being made from nickel and an oxide-reacting material such as Titanium or Tantalum. The next step (6) involves annealing the nickel alloy layer and the substrate causing the nickel in the nickel alloy layer to react with the silicon substrate and form a nickel silicide layer on the substrate surface. By using a nickel alloy containing an oxide-reacting material, silicon oxide, if present on the substrate surface, does not substantially inhibit the formation of the nickel silicide layer.

WO 2003/096407 A1

SE, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) **Designated States** *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designation US*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for the following designation US*

Published:

— *with international search report*

(48) **Date of publication of this corrected version:**
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see PCT Gazette No. 14/2004 of 1 April 2004, Section II

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